

1. why we need testbench in verilog

Test bench is a code written in any HVL Hardware Verification Language (VHDL/VERILOG/SV) to verify if the design works properly.

A test bench is HDL code that allows to provide a documented, repeatable set of stimuli that is portable across different simulators. A test bench can be as simple as a file with clock and input data or a more complicated file that includes error checking, file input and output, and conditional testing.

1. what is the role of file register in mips

* A register file is a small set of high-speed storage cells inside the CPU
* MIPS register file includes 32 32-bit general purpose registers
* This register file makes possible to simultaneously read from two registers and write into one register as it is appropriate for MIPS processor.

1. Slt : Set If Less Than

* The SLT instruction sets the destination register's content to the value 1 if the first source register's contents are  
  less than the second source register's contents. Otherwise, it is set to the value 0.
* It's syntax is:  
  **SLT $destination register's address, $first source register's address, $second source register's address**.
* The sample SLT instruction demonstrated in the datapath above is **SLT $17, $19, $22**.